

Figure 1

The diagram illustrates a dual-port memory system. On the left, the **write control logic** (103) receives an **overflow** signal (107), a **lock write** signal (109), and an **X6XS clock** (74). It outputs a **write address** and **write control** signals to the **DPRAM** (101). The **DPRAM** consists of eight banks (Bank I to Bank VIII), each with an address (109). A **clock domain transition** signal is connected to the bottom of the DPRAM. On the right, the **read control logic** (105) receives an **underflow** signal (111), a **lock read** signal (113), and a **PMA clock** (80). It outputs a **read address** and **read control** signals to the **DPRAM**. The **DPRAM** outputs a **data out** signal (106) to a **2:1 multiplexer** (104). The multiplexer also receives an **error** signal (110) and an **L/F** signal (106). The multiplexer outputs a **data out** signal (104). Handwritten annotations include '75' with an arrow pointing to the read control logic, '76' with an arrow pointing to the data path between the control logic and the DPRAM, and '101' with an arrow pointing to the DPRAM block.

Figure 3

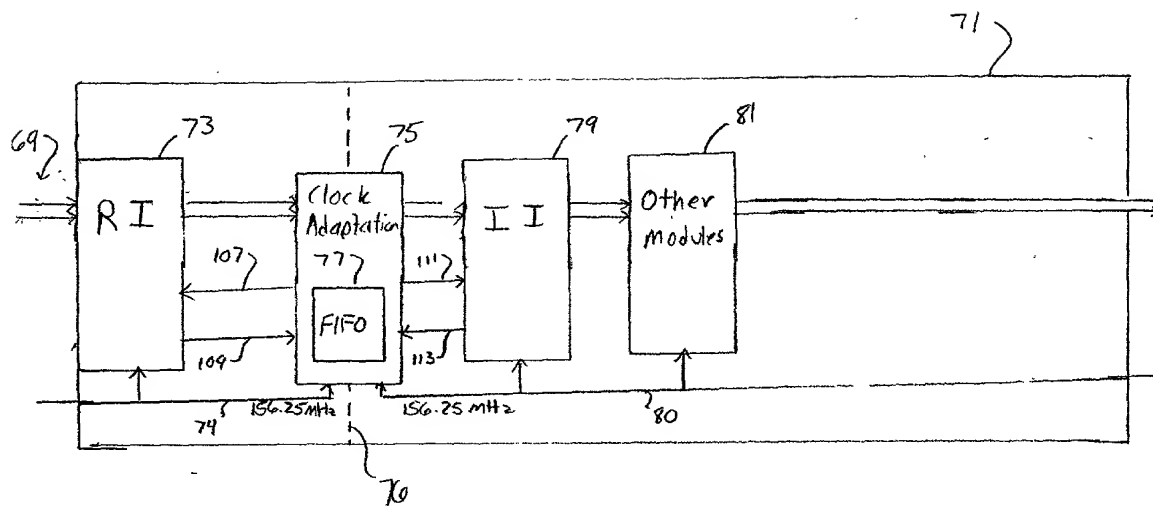


Fig. 2

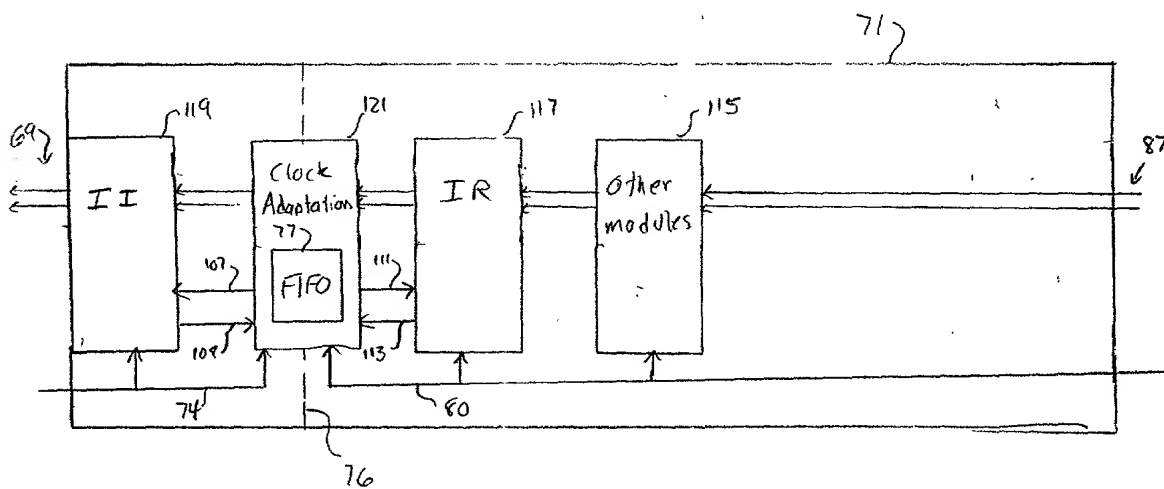


Fig. 4